NETWORK FOR DECREASING TRANSMIT LINK LAYER CORE SPEED

ABSTRACT

A processor includes a core for providing speed reduction in communications between a transmission media and a processor having an upper link layer in a parallel-serial architecture. The core includes a lower logic layer, serial lanes connecting the logic layer to the transmission media, at least one selector connected to the serial lanes for supporting at least two differing data widths. The logic layer controls the selector, and multiple buffers are interposed in the serial lanes. The selector enables the speed reductions is the upper link layer of the processor. The processor is particularly applicable to interface components used in InfiniBand-type hardware.